2. (Once amended) The method for manufacturing a semiconductor device of claim 1 further comprising forming third contact holes by slightly etching a portion of the capping layer exposed by the second contact holes before forming the conductive layer, and wherein the conductive layer is formed within the second contact holes and the third contact holes.

3. The method for manufacturing a semiconductor device of claim 2, wherein the conductive layer is formed only in the second and third contact holes.

4. The method for manufacturing a semiconductor device of claim 2, wherein the conductive layer is an upper interconnection layer filling the second and third contact holes and covering the top surface of the interlayer insulating layer.

5. The method for manufacturing a semiconductor device of claim 2 wherein the second and third contact holes are formed by performing a dry etching method using an etchant having a low etching selectivity between the etching stopper and the capping layer.

6. The method for manufacturing a semiconductor device of claim 1, wherein the etching stopper is formed of an inorganic anti-reflecting layer (ARL) or an organic anti-reflecting coating (ARC).

7. The method for manufacturing a semiconductor device of claim 1, wherein the interconnection layer is a metal layer containing aluminum.

8. The method for manufacturing a semiconductor device of claim 1, wherein the capping layer is formed of TiN, Ti/TiN or TaN.

9. The method for manufacturing a semiconductor device of claim 1, wherein the interlayer insulating layer is formed of one selected from the group consisting of a silicon oxide layer, a silicon nitride layer, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), tetraethylorthosilicate (TEOS), plasma enhanced TEOS (PE-TEOS), and undoped silicate glass (USG).

10. The method for manufacturing a semiconductor device of claim 1, wherein the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers for forming the interconnection layer, the capping layer, and the etching stopper, and patterning the material layers by the same etching process.

11. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is formed only in the second contact holes.

12. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is an upper interconnection layer filling the second contact holes and covering the top surface of the interlayer insulating layer.

13. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the first contact holes are formed by using a dry etching method.

14. (New) The method for manufacturing a semiconductor device of claim 1, wherein the capping layers are etched to form a uniform thickness among the second contact holes.

15. (new) The method for manufacturing a semiconductor device of claim 1, wherein the second contact holes expose a top surface of the capping layers.

16. (New) A method for manufacturing a semiconductor device, the method comprising:

forming plural interconnection layers, each including a material layer comprising a capping layer and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection layers;

forming contact holes to expose a surface of the etching stopper in the interlayer insulating layer;

selectively removing the material layer within the contact holes in such a manner that the capping layers within the contact holes are of uniform thickness; and

forming a conductive layer within the contact holes.

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24.

17. (New) The method for manufacturing a semiconductor device of claim 16, wherein the capping layers are etched to form a uniform thickness in the contact holes.

25.

18. (New) The method for manufacturing a semiconductor device of claim 16, wherein the contact holes expose a top surface of the capping layers.